UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/069,352	08/07/2002	Gilbert Wolrich	10559-308US1	7931

20985 7590 01/30/2007
FISH & RICHARDSON, PC
P.O. BOX 1022
MINNEAPOLIS, MN 55440-1022

EXAMINER	
HUISMAN, DAVID J	
ART UNIT	PAPER NUMBER
2183	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/30/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/069,352	WOLRICH ET AL.	
	Examiner	Art Unit	
	David J. Huisman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 November 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-11,13,14,16,17,20-25,27-30,32,33,35 and 36* is/are rejected.

7)☒ Claim(s) *7,12,15,18,19,26,31,34,37 and 38* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 June 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-38 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment as received on 11/21/2006.

Oath/Declaration

3. The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

The oath or declaration is defective because: It does not identify the citizenship of each inventor. Specifically, in the oath/declaration filed on August 7, 2002, the citizenship for Donald F. Hooper has been omitted.

Drawings

4. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the features of claims 1 and 7-11 must be shown or canceled from the claim(s). None of the subject matter from these claims is illustrated. No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing

sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Withdrawn Rejections

5. Applicant, by way of amendment, has overcome the prior art rejections set forth in the previous Office Action. Consequently, these rejections are hereby withdrawn by the examiner. However, upon further consideration, new grounds of rejection are applied below.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an

> international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1-2, 5-6, 8-10, 20-21, 24-25, and 27-29 are rejected under 35 U.S.C. 102(e) as being anticipated by Barry et al., U.S. Patent No. 6,446,190 (herein referred to as Barry).

8. Referring to claim 1, Barry has taught a method of operating a processor comprising:

a) receiving data specified by execution of a fast-write instruction in a processing thread identified by a processing thread number. See column 9, lines 52-58, and Fig.7A. Note that the fast-write instruction is equivalent to the LIM (Load Immediate) instruction. Also, Barry mentions that context switches occur. Therefore, the system includes multiple threads, and threads are inherently numbered in some way so that they may be identified when switching occurs.

b) the fast-write instruction further specifying a register, the register having multiple groups of bits, each group of bits associated with one of multiple thread available on the processor. See Fig.7A, and column 9, lines 32-36, and note that the LIM instruction specifies a register to be loaded. The register has multiple groups of bits, the first group being the upper 16 bits, and the second group being the lower 16 bits. Since a thread will include the LIM instruction (threads comprise instructions), each group of bits will be associated with the current thread, which is one of multiple threads.

c) selecting a group of bits associated with the processing thread, the group of bits being selected from the multiple groups of bits of the register specified by the fast-write instruction according to the processing thread number. See Fig.7A, and note that if thread 0 (0 being the thread number) includes a LIM instruction that has LOC bits equal to 00 or 01, then either the upper or lower group of bits will be selected. This selection is done according to processing thread number as

thread 0 contains the LIM instruction. That is, in response to thread 0 being executed, a group of bits from the register will be selected (due to the thread having the LIM instruction).

d) loading the data into the selected bit positions of the register. See Fig.7A, and note that when LOC = 00 or 01, the group is loaded with the immediate data supplied in the LIM instruction.

9. Referring to claim 2, Barry has taught a method as described in claim 1. Barry has further taught that the register is a control and status register (CSR). See column 9, lines 32-33.

10. Referring to claim 5, Barry has taught a method as described in claim 1. Barry has further taught that the data represents hexadecimal mask values 0 to 0x3FF. See Fig.7A, and column 9, lines 52-58, and note that a group comprises 16 bits and so the data written to a given group may range from 0 to 0xFFFF, which includes the range 0 to 0x3FF.

11. Referring to claim 6, Barry has taught a method as described in claim 1. Barry has further taught that the processing thread represents processing in a micro engine of a multithreaded processor. See column 9, lines 52-58 and recall that Barry performs context switches and therefore has multiple threads and is a multithreaded processor. A unit that performs execution on a multithreaded processor is a "micro-engine," i.e., execution unit.

12. Referring to claim 8, Barry has taught a method as described in claim 1. Barry has further taught that the fast-write instruction comprises a token. See Fig.7A. The token comprises at least one of the groups that make up the fast-write instruction. The token could also be interpreted as being all 32 bits of the instruction.

13. Referring to claim 9, Barry has taught a method as described in claim 8. Barry has further taught that the token represents overriding qualifiers. Since the instruction writes to a register using the data provided in the instruction, each bit of the data represents an overriding

qualifier as each "old" bit of the selected group in the register will be overridden by each respective "new" bit of the data.

14. Referring to claim 10, Barry has taught a method as described in claim 8. Barry has further taught that the token is a 32-bit word. See Fig.7A. The token comprises at least one of the groups that make up the fast-write instruction. The token could also be interpreted as being all 32 bits of the instruction.

15. Referring to claims 20-21, 24-25, and 27-29, claims 20-21, 24-25, and 27-29 are rejected for the same reasons set forth in the rejection of claims 1-2, 5-6, and 8-10, respectively, because Barry has taught instructions stored on a medium for performing the method of claims 1-2, 5-6, and 8-10.

16. Claims 1-2, 6, 8-9, 20-21, 25, and 27-28 are rejected under 35 U.S.C. 102(e) as being anticipated by Velingker, U.S. Patent No. 6,279,066.

17. Referring to claim 1, Velingker has taught a method of operating a processor comprising:

a) receiving data specified by execution of a fast-write instruction in a processing thread identified by a processing thread number. See Figs.2-4 and column 5, lines 19-50. Note from Fig.3 that multiple processors each execute different threads (threads 1, 2, and 3). When a thread wants access to a shared resource, it issues an instruction (fast-write instruction) to set a bit in the RNC (register)

b) the fast-write instruction further specifying a register, the register having multiple groups of bits, each group of bits associated with one of multiple thread available on the processor. See Figs.2-3, column 5, lines 19-50, and column 6, lines 10-18. In one embodiment of the invention,

the resource negotiation cell (RNC) is a register with three groups of bits, each group comprising two bits (a request bit and a completion bit). Each group is associated with a different thread. When a thread wants to request a resource or indicate access completion, a fast-write instruction including data is issued to set an appropriate bit in the corresponding group.

c) selecting a group of bits associated with the processing thread, the group of bits being selected from the multiple groups of bits of the register specified by the fast-write instruction according to the processing thread number. Again, see column 5, lines 19-50, column 6, lines 10-18, and Figs.2-3. When a thread wants to access a shared resource or indicate access completion, the thread's group of bits is selected for modification.

d) loading the data into the selected bit positions of the register. See column 5, lines 19-50, column 6, lines 10-18, and Figs.2-3. When the thread wants to access a shared resource, it will write a '1' into a bit of the group of bits. And, when it is finished accessing the resource, it will write a '1' into another bit of the group of bits.

18. Referring to claim 2, Velingker has taught a method as described in claim 1. Velingker has further taught that the register is a control and status register (CSR). See Fig.3. The register written to controls (and specifies the status of) shared resource access.

19. Referring to claim 6, Velingker has taught a method as described in claim 1. Velingker has further taught that the processing thread represents processing in a micro engine of a multithreaded processor. See Fig.1, and note that each processor (micro engine) processes a thread.

20. Referring to claim 8, Velingker has taught a method as described in claim 1. Velingker has further taught that the fast-write instruction comprises a token. See column 5, lines 19-50,

and note that an instruction having a form equivalent to "WRITE REQUEST 1" will be issued. This instruction will write a '1' to the access bit. The '1' is the token.

21. Referring to claim 9, Velingker has taught a method as described in claim 8. Velingker has further taught that the token represents overriding qualifiers. Since the instruction writes to a register bit using the data provided in the instruction, the bit of the data (token) represents an overriding qualifier as the "old" bit of the selected group in the register will be overridden by the "new" data.

22. Referring to claims 20-21, 25, and 27-28, claims 20-21, 25, and 27-28 are rejected for the same reasons set forth in the rejection of claims 1-2, 6, and 8-9, respectively, because Velingker has taught instructions stored on a medium for performing the method of claims 1-2, 6, and 8-9.

Claim Rejections - 35 USC § 103

23. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

24. Claims 3-4, 11, 13-14, 16-17, 22-23, 30, 32-33, and 35-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Barry.

25. Referring to claim 3, Barry has taught a method as described in claim 2. Barry has not explicitly taught that the control and status register is coupled to a 64-bit wide first-in first-out (FIFO) bus. However, as shown in *In re Rose, 105 USPQ 237 (CCPA 1955)*, changes in size are generally not given patentable weight or would have been an obvious improvement.

Specifically, the size of Barry's bus appears to be 32 bits (see Fig.1A). However, a 64-bit bus is a common bus size that allows for more data to be transported at once than on a 32-bit bus. Consequently, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Barry's bus to be 64-bits wide. Furthermore, the bus is inherently FIFO because data that is sent over the bus at time A will arrive at its destination before data that is sent over the bus at time B (where B > A).

26. Referring to claim 4, Barry has taught a method as described in claim 3. Furthermore, it is deemed inherent in Barry that the FIFO bus interfaces with Media Access Controller (MAC) devices. There must be devices which control the means for communicating across a bus. These devices are media access controllers as they control media access.

27. Referring to claim 11, Barry has taught a method as described in claim 10. Barry has further taught that a token format comprises data in bits 31:0 (see Fig.7A). Barry has not explicitly taught that the data in bit 31 corresponds to an OV field, the data in bits 30:28 corresponds to a micro engine (UENG) ADDR field, the data in bits 27:16 corresponds to a reserved field, the data in bit 15 corresponds to an OV field, the data in bits 14:5 corresponds to a fast write data field, the data in bits 4:3 corresponds to a reserved field, the data in bit 2 corresponds to an OV field, and the data in bits 1:0 corresponds to a CTX field. However, these differences are only found in the nonfunctional descriptive material as the dividing up of the token bits into named fields does not affect how the token data is used to control the system. For instance, bit 31 of the token in Fig.7A of Barry has a meaning in the system whether or not it is called an OV field. Thus, the descriptive material will not distinguish the claimed invention from the prior art in terms of patentability. See *In re Gulack, 703 F.2d 1381, 1385, 217 USPQ*

401, 404 (Fed. Cir. 1983); In re Lowry, 32 F.3d 1579, 32, USPQ2d 1031 (Fed. Cir. 1994). Therefore, it would have been obvious to a one of ordinary skill in the art at the time of the invention to call a bit or any group of bits in the token a particular type of field as it does not alter how the data controls the system. Applicant should explain what each field does in order to overcome the prior art.

28. Referring to claim 13, Barry has taught a method as described in claim 11. Barry has further taught that bits 30:28 specify a micro engine associated with a control and status register (CSR). See column 9, lines 52-58, and Fig.7A, and note that bits 30:28 include bit 29, which is an S/P bit. This bit specifies whether a register of an SP or a PE (the micro engines shown in Fig.1A) is modified.

29. Referring to claim 14, Barry has taught a method as described in claim 11. Barry has further taught that bits 27:16 return 0 when read. That is, if bits 27:16 are all set to 0 (which is a possible combination since all bits are set to 0 or 1), then when read, the value 0 would be obtained.

30. Referring to claim 16, Barry has taught a method as described in claim 11. Barry has further taught that bits 14:5 represent valid data to be written to a control and status register (CSR). See Fig.7A, and note that bits 15:0, which include bits 14:5 are written to the register.

31. Referring to claim 17, Barry has taught a method as described in claim 11. Barry has further taught that bits 4:3 return 0 when read. That is, if bits 4:3 are all set to 0 (which is a possible combination since all bits are set to 0 or 1), then when read, the value 0 would be obtained.

32. Referring to claims 22-23, 30, 32-33, and 35-36, claims 22-23, 30, 32-33, and 35-36 are rejected for the same reasons set forth in the rejection of claims 3-4, 11, 13-14, and 16-17, respectively, because Barry has taught instructions stored on a medium for performing the method of claims 3-4, 11, 13-14, and 16-17.

33. Claims 3-4 and 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Velingker.

34. Referring to claim 3, Velingker has taught a method as described in claim 2. Velingker has not explicitly taught that the control and status register is coupled to a 64-bit wide first-in first-out (FIFO) bus. However, as shown in *In re Rose, 105 USPQ 237 (CCPA 1955)*, changes in size are generally not given patentable weight or would have been an obvious improvement. Specifically, the size of Velingker's bus is not disclosed, but a 64-bit bus is a common bus size, which allows for more data to be transported at once than on a 32-bit bus or 16-bit bus, for instance. Consequently, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Velingker's bus to be 64-bits wide. Furthermore, the bus is inherently FIFO because data that is sent over the bus at time A will arrive at its destination before data that is sent over the bus at time B (where B > A).

35. Referring to claim 4, Velingker has taught a method as described in claim 3. Furthermore, it is deemed inherent in Velingker that the FIFO bus interfaces with Media Access Controller (MAC) devices. There must be devices which control the means for communicating across a bus. These devices are media access controllers as they control media access.

36. Referring to claims 22-23, claims 22-23 are rejected for the same reasons set forth in the rejection of claims 3-4, respectively, because Velingker has taught instructions stored on a medium for performing the method of claims 3-4.

Allowable Subject Matter

37. Claims 7, 12, 15, 18-19, 26, 31, 34, and 37-38 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

38. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David J. Huisman whose telephone number is (571) 272-4168. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DJH
David J. Huisman
December 15, 2006

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100